## AMENDMENTS TO THE CLAIMS
(with complete listing)

1-113. (Cancelled)

114. (New) A sensor array (18′) comprising:

first and second sensor pods (12′) each characterized by having a sensor (126) therein operatively coupled to a multiple-bit memory (28′) structured for storing data therefrom, a processor (120) operatively coupled to said memory (28′), a first node (72) in bi-directional communication with said memory (28′) via a first communications converter (112), a second node (74) in bi-directional communication with said memory (28′) via a second communications converter (114), and a choke (106) electrically connected between said first node (72) and said second node (74);

a telemetry and control module (21′);

a first cable connected between said telemetry and control module (21′) and said first sensor pod (12′), said first cable including an electrical conductor that is connected between said telemetry and control module (21′) and said first node (72) of said first sensor pod (12′); and

a second cable connected between said first sensor pod (12′) and said second sensor pod (12′), said second cable including an electrical conductor that is connected between said second node (74) of said first sensor pod and said first node (72) of said second sensor pod;

a first signal path disposed between said telemetry and control module (21′) and said memory (28′) of said first sensor pod (12′) including said electrical conductor of said first cable, said first node (72) of said first sensor pod (12′), and said first communications converter (112) of said first sensor pod (12′);

a second signal path disposed between said memory (28′) of said first sensor pod (12′) and said memory (28′) of said second sensor pod (12′) including said second communications

converter (114) of said first sensor pod (12′), said second node (74) of said first sensor pod (12′), said conductor of said second cable, said first node (72) of said second sensor pod (12′), and said first communications converter (112) of said second sensor pod (12′); and

a direct current power pathway disposed between said telemetry and control module (21′) and said first and second sensor pods (12′) including said conductor of said first cable, said first node (72) of said first sensor pod (12′), said choke (106) of said first sensor pod (12′), said second node (74) of said first sensor pod (12′), said conductor of said second cable, said first node (72) of said second sensor pod (12′), said choke (106) of said second sensor pod (12′), and said second node (74) of said second sensor pod (12′).

115. (New) The sensor array of claim 114 wherein:

each of said first and second sensor pods (12′) is arranged to simultaneously transfer first data from said memory (28′) to said first node (72) and second data from said second node (74) to said memory (28′).

116. (New) The sensor array of claim 114 further comprising:

first pod data disposed in said memory (28′) of said first sensor pod (12′) at a first point in time;

second pod data disposed in said memory (28′) of said second sensor pod (12′) at said first point in time;

said first pod data disposed in a memory element of said telemetry and control module (21′) at a second point in time after said first point; and

said second pod data disposed in said memory (28′) of said first sensor pod (12′) at said second point in time.

117. (New) The sensor array of claim 116 further comprising:

said second pod data disposed in said memory element of said telemetry and control module (21′) at a third point in time after said second point.

118. (New) The sensor array of claim 114 further comprising:

a conductive bypass pathway electrically connected between said first node (72) and said second node (74) in parallel with said choke (106); and

a switch element (132) electrically connected within said bypass pathway;

whereby when said switch element (132) of said first sensor pod (12′) is closed, a third signal path is established between said telemetry and control module (21′), said memory (28′) of said first sensor pod (12′), and said memory (28′) of said second sensor pod (12′), said third signal path including said conductor of said first cable, said first node (72) of said first sensor pod (12′), said first communications converter (112) of said first sensor pod (12′), said bypass pathway of said first sensor pod (12′), said second node (74) of said first sensor pod (12′), said conductor of said second cable, said first node (72) of said second sensor pod (12′), and said first communications converter (112) of said second sensor pod (12′).

119. (New) The sensor array of claim 118 wherein:

each of said first and second sensor pods (12′) further includes a first direct current block (116) electrically connected between said first node (72) and said first communications converter (112) and a second direct current block (118) electrically connected between said second node (74) and said second communications converter (114).

120. (New) The sensor array of claim 118 wherein:

each of said first and second sensor pods (12′) further includes a power supply module (108) electrically connected to said choke (106).